It is claimed:

1. A current steering digital-to-analog (DAC), comprising:

a plurality of current steering segments each comprising differential transistors to steer a current from a summing node to either a positive output or a negative output of said DAC; and

a control circuit to reduce a variation of a voltage present at the summing node of each of said current steering segments.

2. The current steering DAC of claim 1, wherein said control circuit comprises a first control circuit to reduce said variation of said voltage present at the summing node of each of said current steering segments steering current to said positive output in response to a voltage present at said positive output.

3. The current steering DAC of claim 2, wherein said control circuit comprises a second control circuit to reduce said variation of said voltage present at the summing node of each of said current steering segments steering current to said negative output in response to a voltage present at said negative output.

4. The current steering DAC of claim 2, wherein said first control circuit comprises:

an operational amplifier including first and second input terminals and an output terminal, wherein said output terminal is electrically connected to a substrate terminal of the differential transistor, that is electrically connected to the positive output, of each of said current steering segments;

a reference voltage source electrically connected to said first input terminal of said operational amplifier; and

a transistor including a first terminal electrically connected to said second input terminal of said operational amplifier, a second terminal electrically connected to said positive output, a control terminal electrically connected to a constant-voltage terminal, and a substrate terminal electrically connected to said output terminal of said operational amplifier.

5. The current steering DAC of claim 4, wherein said transistor comprises fingers of substantially the same length and width as the differential transistors that are electrically connected to said positive output of said DAC.

6. The current steering DAC of claim 4, wherein said transistor is configured to have substantially the same drain current as the differential transistors that are electrically connected to said positive output of said DAC.

7. The current steering DAC of claim 4, wherein said first input terminal of said operational amplifier comprises a positive input terminal of said operational amplifier, and said second input terminal of said operational amplifier comprises a negative input terminal of said operational amplifier.

8. The current steering DAC of claim 4, wherein said reference voltage source comprises a diode-connected transistor electrically connected between said first input terminal and said constant-voltage terminal.

9. The current steering DAC of claim 8, wherein said transistor and said diode-connected transistor are FETs, and wherein said diode-connected transistor is substantially the same size and configured to have substantially the same drain current as said transistor.

10. The current steering DAC of claim 8, wherein said diode-connected transistor comprises a field effect transistor (FET).

11. The current steering DAC of claim 4, wherein said transistor comprises a field effect transistor (FET).

12. The current steering DAC of claim 11, wherein said first terminal of said FET comprises a source terminal of said FET, said second terminal of said FET

comprises a drain terminal of said FET, and said control terminal of said FET comprises a gate terminal of said FET.

13. The current steering DAC of claim 4, wherein said constant-voltage terminal comprises a ground terminal.

14. The current steering DAC of claim 3, wherein said second control circuit comprises:

an operational amplifier including first and second input terminals and an output terminal, wherein said output terminal is electrically connected to a substrate terminal of the differential transistor, that is electrically connected to the negative output, of each of said current steering segments;

a reference voltage source electrically connected to said first input terminal of said operational amplifier; and

a transistor including a first terminal electrically connected to said second input terminal of said operational amplifier, a second terminal electrically connected to said negative output, a control terminal electrically connected to a constant-voltage terminal, and a substrate terminal electrically connected to said output terminal of said operational amplifier.

15. The current steering DAC of claim 14, wherein said transistor comprises fingers of substantially the same length and width as the differential transistors that are electrically connected to said negative output of said DAC.

16. The current steering DAC of claim 14, wherein said transistor is configured to have substantially the same drain current as the differential transistors that are electrically connected to said negative output of said DAC.

17. The current steering DAC of claim 14, wherein said first input terminal of said operational amplifier comprises a positive input terminal of said operational amplifier, and said second input terminal of said operational amplifier comprises

a negative input terminal of said operational amplifier.

18. The current steering DAC of claim 14, wherein said reference voltage source comprises a diode-connected transistor electrically connected between said first input terminal and said constant-voltage terminal.

19. The current steering DAC of claim 18, wherein said transistor and said diode-connected transistor are FETs, and wherein said diode-connected transistor is substantially the same size and configured to have substantially the same drain current as said transistor.

20. The current steering DAC of claim 18, wherein said diode-connected transistor comprises a field effect transistor (FET).

21. The current steering DAC of claim 14, wherein said transistor comprises a field effect transistor (FET).

22. The current steering DAC of claim 21, wherein said first terminal of said FET comprises a source terminal of said FET, said second terminal of said FET comprises a drain terminal of said FET, and said control terminal of said FET comprises a gate terminal of said FET.

23. The current steering DAC of claim 14, wherein said constant-voltage terminal comprises a ground terminal.

24. The current steering DAC of claim 1, wherein said control circuit comprises a first control circuit to reduce said variation of said voltage present at the summing node of each of said current steering segments steering current to said negative output in response to a voltage present at said negative output.

25. The current steering DAC of claim 1, wherein each of said current steering

segments comprises a current-setting transistor for setting said current through said corresponding current setting transistor.

26. The current steering DAC of claim 25, wherein each of said current steering segments comprises a cascode transistor for setting a drain-to-source voltage of said corresponding current steering segment.

27. The current steering DAC of claim 1, further comprising a thermometer code decoder to generate signals for controlling the current steering of each of said current steering segments in response to an input digital signal.

28. A method of converting an input digital signal to a differential analog output signal, comprising:

steering currents from respective summing nodes to positive and/or negative outputs in response to said input digital signal to generate said differential analog output signal; and

reducing variations of voltages present respectively at said summing nodes.

29. The method of claim 28, wherein reducing said variations of voltages present respectively at a portion of said summing nodes comprises:

sensing a variation of a voltage at said positive output; and

reducing said variations of the voltages at said portion of said summing nodes in response to said variation of said voltage at said positive output.

30. The method of claim 28, wherein reducing said variations of the voltages at said portion of said summing nodes comprises:

comparing said voltage at said positive output with a substantially constant voltage; and

reducing said variations of the voltages at said portion of said summing nodes in response to an outcome of said comparison.

31. The method of claim 28, wherein steering currents from respective summing nodes to positive and/or negative outputs comprises employing differential transistors to steer said currents from respective summing nodes.

32. The method of claim 31, wherein reducing said variations of the voltages at said portion of said summing nodes in response to said variation of said voltage at said positive output comprises controlling a threshold voltage of one or more differential transistors electrically connected to said positive output.

33. The method of claim 32, wherein controlling said threshold voltage of one or more differential transistors electrically connected to said positive output comprises:

generating a differential voltage responsive to a difference between said voltage at said positive output and a substantially constant voltage; and

controlling said threshold voltage of one or more differential transistors electrically connected to said positive output using said differential voltage.

34. The method of claim 28, wherein reducing said variations of said voltages present respectively at a portion of said summing nodes comprises:

sensing a variation of a voltage at said negative output; and

reducing said variation of the voltages at said portion of said summing nodes in response to said variation of said voltage at said negative output.

35. The method of claim 34, wherein reducing said variations of the voltages said portion of said summing nodes comprises:

comparing said voltage at said negative output with a substantially constant voltage; and

reducing said variations of the voltages at a portion of said summing nodes in response to an outcome of said comparison.

36. The method of claim 28, wherein steering currents from respective summing nodes to positive and/or negative outputs comprises employing differential transistors to steer said currents from respective summing nodes.

37. The method of claim 36, wherein reducing said variations of the voltages at said portion of said summing nodes in response to said variation of said voltage at said negative output comprises controlling a threshold voltage of one or more differential transistors electrically connected to said negative output.

38. The method of claim 37, wherein controlling said threshold voltage of one or more differential transistors electrically connected to said negative output comprises:

generating a differential voltage responsive to a difference between said voltage at said negative output and a substantially constant voltage; and

controlling said threshold voltage of one or more differential transistors electrically connected to said negative output using said differential voltage.

39. The method of claim 28, further comprising setting and controlling respective steering currents.

40. The method of claim 28, further comprising adjusting respective output impedances of said positive and negative outputs.